

Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-16 are pending in the application, with claims 1 and 12 being the independent claims. By this amendment, Applicant seeks to amend claims 1, 8, and 12. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Applicants believe the amendments should be entered after final because they require no further search or consideration, as the Examiner has already examined these features, and because they place the application in condition for allowance and/or better condition for appeal.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Examiner Interview

Applicants respectfully thank the Examiner for extending the courtesy of a telephone interview to Applicants' representatives on March 31, 2009. Applicants' representatives found the Examiner's comments very helpful and instructive.

Rejections Under 35 U.S.C. § 102

Claims 1-4, 6, 8-14, and 16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by CS4205 (CrystalClear Audio Codec '97 product information document, hereinafter "CrystalClear"). Applicants traverse the rejection of claims 1-4, 6, 8-14, and 16 because the cited reference fails to disclose, teach, or suggest all of the features of the claimed invention.

For example, CrystalClear fails to disclose, teach, or suggest:

"A method for communicating audio, comprising: communicating audio using a 2-line serial multi-channel audio interconnect data bus including only a first signal line and a second signal line... wherein only the first signal line and the second signal line form the 2-line serial multi-channel audio interconnect data bus structured to communicate audio."

as recited, for example, in claims 1 and 12. These features are discussed, for example, in Applicants' specification in paragraphs 0026 to 0028, and are illustrated in FIG. 2.

By contrast, CrystalClear audio interfaces are formed by at least three wires/lines including a clock line, a data line, and a sync line (see, e.g., FIG. 14), not only a first signal line and a second signal line, as recited in Applicants' claims. The CS4205 audio codec communicates with two main components: a DC '97 controller and stereo ADCs/DACs (see figure 16). As stated in CrystalClear, the DC '97 (also known as the Digital AC '97) controller "is responsible for all communications between the CS4205 and the remainder of the system" (see section 2, page 13). And as stated in CrystalClear, "all communication with the CS4205 is established with a **5-wire digital interface** to the controller called the AC-link" (see section 2.1, page 13). That is, in CrystalClear, five lines form the AC-link interface, including a required clock line BIT_CLK, SYNC, and SDATA. This is illustrated in FIGS. 7 and 14. CrystalClear further discloses that "all clocking for the serial communication is synchronous to the BIT_CLK," and the "BIT_CLK is generated by the primary audio codec and is used to clock the controller and any secondary audio codecs" (see section 2.1, page 13; see also page 72 defining the SDATA_OUT and SDATA_IN lines in terms of BIT_CLK clocking the data in/out on rising/falling edges of the clock). Thus CrystalClear fails to disclose communicating audio using a data bus including only a first signal line and a second signal line.

More specifically, CrystalClear teaches that the AC-link interface requires a clock line (see section 4, page 19, figure 14); **BIT CLK**. Because the CS4205 audio codec generates its own clock signal and all communication is synchronous with this clock signal, the CS4205 audio codec must transmit this clock signal, BIT_CLK, to all relevant components interfacing via AC-link. Figure 14 illustrates the serial port timing during both serial data output and input frames as noted in the first paragraph of section 4.1 and the first paragraph of section 4.2. At least one line is required for SDATA, and at least one line is required for SYNC, thus at least three lines are required for an interface or bus transmitting audio in CrystalClear.

CrystalClear further teaches additional interfaces, but the additional interfaces similarly require at least three lines for communicating audio. Digital Docking interface (CrystalClear page 54, section 6.3 and FIG. 16), includes at least three wires/lines and requires a clock line (SCLK and/or LRCLK). CrystalClear teaches Serial Data Formats (CrystalClear section 6.4; FIGS. 17-20), wherein the interfaces (e.g., I²S of FIG. 17) include at least three wires/lines and requiring a clock line (SCLK). Additionally, even the asynchronous ZV Port (CrystalClear section 7; FIG. 21) requires a clock line ZSCLK in conformance with the use of an I²S interface as taught in CrystalClear section 7 (the I²S interface is additionally distinguished in, for example, paragraphs 5-6 of the present application).

Thus, Applicants submit that the various audio interfaces of CrystalClear require three or more lines including a clock line, in contrast to presently amended claims 1 and 12 reciting, for example, "communicating audio using a 2-line serial multi-channel audio interconnect data bus including only a first signal line and a second signal line."

It is respectfully pointed out that anticipation can only be established by a single prior art reference that discloses each and every element of the claimed invention. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440 (Fed. Cir. 1984). Therefore, because the cited reference fails to recite each and every element recited in claims 1 and 12, claims 1 and 12 are not anticipated by the cited references and are therefore allowable.

Claims 2-4, 6, and 8-11 depend from claim 1 and claims 13-14, and 16 depend from claim 12. Therefore claims 2-4, 6, 8-11, 13-14, and 16 are allowable at least for the reasons claims 1 and 12 are allowable, and for the specific features recited therein.

Rejections Under 35 U.S.C. § 103

Claims 5 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over CrystalClear in view of U.S. Patent No. 7,088,398 to Wolf et al. (hereinafter "Wolf"). Wolf fails to overcome the deficiencies of CrystalClear relative to claims 1 and 12, described above. Claims 5 and 15 depend from claims 1 and 12 respectively, and are allowable at least for the reasons claims 1 and 12 are allowable. For at least these reasons and further in view of their own features, claims 5 and 15 are patentable over the combination of CrystalClear and Wolf. Reconsideration and withdrawal of the ground of rejection is therefore respectfully requested.

Claim 7 stands rejected under 35 U.S.C. § 103 (a) as being unpatentable over CrystalClear in view of U.S. Patent No. 6,006,287 to Wakazu (hereinafter "Wakazu"). Claim 7 depends ultimately from claim 1. Wakazu does not overcome all of the deficiencies of CrystalClear relative to claim 1, described above. For at least these reasons and further in view of their own features, claim 7 is patentable over the

combination of CrystalClear and Wakazu. Reconsideration and withdrawal of the ground of rejection is therefore respectfully requested.

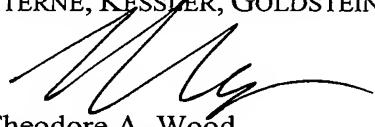
Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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